

AMENDMENTS -- CLEAN VERSION

Presented below are the amendments in a clean, unmarked format with changes entered and not marked.

In the Claims:

46. (New) --A method comprising:

receiving a signal pulse; and

in response to the signal pulse:

pulling a voltage of a first drain bias circuit for a non-volatile memory cell

to a voltage potential of a voltage source;

pulling a voltage of a second drain bias circuit of a reference cell to the

voltage potential of the voltage source; and

shorting a sense node for the non-volatile memory cell to a reference node

for the reference cell.--

47. (New) --The method of claim 46, wherein the non-volatile memory cell

comprises a flash memory cell.--

48. (New) --The method of claim 46, wherein:

pulling the voltage of the first drain bias circuit to the voltage potential of the

voltage source comprises enabling a first kicker device coupled to the first  
drain bias circuit; and

pulling the voltage of the second drain bias circuit to the voltage potential of the

voltage source comprises enabling a second kicker device coupled to the  
second drain bias circuit.--

49. (New) --The method of claim 48, wherein the first kicker device and the second kicker device each comprise a high performance transistor.--
50. (New) --The method of claim 46, wherein shorting the sense node to the reference node comprises enabling a semiconductor device coupled between the sense node and the reference node.--
51. (New) --The method of claim 50, wherein enabling the semiconductor device coupled between the sense node and the reference node equalizes a voltage potential of the sense node with a voltage potential of the reference node during bit charging.--
52. (New) --The method of claim 51, further comprising:  
pulling the voltage potential of the sense node to the voltage potential of the  
voltage source minus the voltage across the first drain bias circuit; and  
pulling the voltage potential of the reference node to the voltage potential of the  
voltage source minus the voltage across the second drain bias circuit.--
53. (New) --The method of claim 46, wherein the signal pulse is received prior to sensing the contents of the non-volatile memory cell.--
54. (New) --The method of claim 46, wherein the first drain bias circuit and the second drain bias circuit each comprise a cascode amplifier.--
55. (New) --A non-volatile memory device comprising:  
a first kicker device, a first terminal of the first kicker device being coupled to a  
voltage source and a second terminal of the first kicker device being

coupled to a first drain bias circuit for a memory cell of the non-volatile memory device;

a second kicker device, a first terminal of the second kicker device being coupled to the voltage source and a second terminal of the second kicker device being coupled to a second drain bias circuit for a reference cell of the non-volatile memory device; and

a semiconductor device, a first terminal of the semiconductor device being coupled to a sense node of the memory cell and a second terminal of the semiconductor device being coupled to a reference node of the reference cell;

in response to a signal pulse:

the first kicker device pulling a voltage of the first drain bias circuit to a voltage potential of the voltage source,

the second kicker device pulling a voltage of the second drain bias circuit to the voltage potential of the voltage source, and

the semiconductor device shorting the sense node with the reference node.

56. (New) --The non-volatile memory device of claim 55, wherein the non-volatile memory device is a flash memory device.--
57. (New) --The non-volatile memory device of claim 55, wherein the signal pulse is received prior to sensing the contents of the memory cell.--

58. (New) --The non-volatile memory device of claim 55, wherein the first kicker device and the second kicker device each comprise a high performance transistor.--
59. (New) --The non-volatile memory device of claim 55, wherein <sup>the</sup> semiconductor device equalizes a voltage potential of the sense node with a voltage potential of the reference node during bit charging.--
60. (New) --The non-volatile memory device of claim 55, wherein the first drain bias circuit and the second drain bias circuit each comprises a cascode amplifier.--
61. (New) --A flash memory device, comprising:
- a memory cell array;
- a reference cell array;
- a first drain bias circuit for a memory cell in the memory cell array and a second drain bias circuit for a reference cell in the reference cell array;
- a first kicker device, a first terminal of the first kicker device being coupled to a voltage source and a second terminal of the first kicker device being coupled to the first drain bias circuit;
- a second kicker device, a first terminal of the second kicker device being coupled to the voltage source and a second terminal of the kicker device being coupled to the second drain bias circuit; and
- a semiconductor device, a first terminal of the semiconductor device being coupled to a sense node of the memory cell and a second terminal of the

semiconductor device being coupled to a reference node of the reference cell;

upon receiving an enable signal:

the first kicker device pulling a voltage of the first drain bias circuit to a

voltage potential of the voltage source,

the second kicker device pulling a voltage of the second drain bias circuit

to the voltage potential of the voltage source, and

the semiconductor device shorting the sense node with the reference node.--

62. (New) --The flash memory device of claim 61, wherein the enable signal is received prior to sensing the contents of the memory cell.--

63. (New) --The flash memory device of claim 61, wherein the first kicker device and the second kicker device each comprises a high performance transistor.--

64. (New) --The flash memory device of claim 63, wherein each high performance transistor is a P-channel semiconductor device.--

65. (New) --The flash memory device of claim 61, wherein the semiconductor device equalizes a voltage potential of the sense node with a voltage potential of the reference node during bit charging.--

66. (New) --The non-volatile memory device of claim 61, wherein the first drain bias circuit and the second drain bias circuit each comprise a cascode amplifier.--

67. (New) --An apparatus comprising:

means for pulling a voltage of a first drain bias circuit for a non-volatile memory cell to a voltage potential of a voltage source in response to an enable signal;

means for pulling a voltage of a second drain bias circuit for a reference memory cell to the voltage potential of the voltage source in response to the enable signal; and

means for shorting a sense node of the non-volatile memory cell to a reference node of the reference cell in response to the enable signal.--

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